REMARKS

New Claims 13-16 have been added. Claims 13 and 14 are identical to Claims 3 and 5, except that Claims 13 and 14 depend from Claim 2. Likewise, Claims 15 and 16 are identical to Claims 9 and 11, except that Claims 15 and 16 depend from Claim 8.

Applicant acknowledges with appreciation the notice of allowable subject matter of Claims 2, 4, 6, 8, 10, and 12, however, Applicant submits that these claims are distinguishable over the prior art of record for reasons not limited to those presented by the examiner, and that the record speaks for itself.

Claims 1-16 are pending in the application.

By way of this response, Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain any outstanding issues that require adverse action, it is respectfully requested that the examiner telephone Timothy R. Croll at (408)433-7625 so that such issues may be resolved as expeditiously as possible.

Response to the rejection under 35 U.S.C. § 103

Claim 1, 3, 5, 7, 9 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Verhelst et al., U.S. Patent 5,057,774 (*Verhelst*) in view of Cole et al., U.S. Patent 6,031,386 (*Cole*). Applicant traverses the rejection as follows.

Claim 1 recites measuring a quiescent current at a first supply voltage and a quiescent current at a second supply voltage for each of a plurality of devices.

The rejection argues in section 2, page 2, that

Verhelst teaches measuring a quiescent current at a first supply voltage and at a second supply voltage for each of a plurality of devices. However, as *Verhelst* explains in column 4, lines 30-38 in FIG. 1A cited by the rejection, what the rejection calls a second supply voltage is in fact not a voltage, rather one of the two supply lines across which the voltage *VDD* is defined. Specifically, the second supply line is defined by *Verhelst* as *VSS*, commonly referred to as ground. In FIG. 5, *Verhelst* shows that *VSS* is indeed the ground reference for the supply voltage *VDD* by including the electrical symbol for ground.

The rejection errs in confusing the second supply line in *Verhelst* with the claimed second voltage. As is well known in the art of electronics, a voltage is defined between two points, one of which is typically a ground reference. Because the second supply line *VSS* in *Verhelst* is only the ground reference for the voltage *VDD*, *VSS* is not a second supply voltage at which a quiescent current is measured as alleged by the rejection. Because *Verhelst* does not teach or suggest the claimed second supply voltage in addition to the first supply voltage recited in Claim 1, the modification of *Verhelst* by *Cole* proposed by the rejection fails to arrive at the claimed invention.

The rejection further errs in alleging that *Verhelst* teaches measuring a quiescent current at a second supply voltage. In column 4, lines 30-38 cited by the rejection, *Verhelst* refers to measuring quiescent current at only one voltage, namely, the supply voltage *VDD*. The supply voltage *VDD* is defined between the first supply line *VDD* and the second supply line *VSS*. As explained above, the second supply line *VSS* is the ground reference for the voltage *VDD*, not a second supply voltage as alleged by the rejection. Further,

Verhelst makes no mention of a quiescent current measurement other than that associated with the supply voltage *VDD*. Because *Verhelst* does not teach measuring quiescent current at a second supply voltage, the modification of *Verhelst* by *Cole* proposed by the rejection fails to arrive at the claimed invention.

The rejection further errs in alleging in section 2, page 3, that *Cole* teaches generating the claimed plot of quiescent current. In column 8, lines 20-51 and FIG. 3 cited by the rejection, *Cole* describes a plot of the supply voltage *VDD* vs. time, not a plot of quiescent current at the supply voltage *VDD* vs. quiescent current at a second supply voltage as described in the specification, shown in FIG. 1, and recited in Claim 1. Because *Cole* does not teach generating the claimed plot of quiescent current, the modification of *Verhelst* by *Cole* proposed by the rejection fails to arrive at the claimed invention.

The rejection further errs in alleging in section 2, page 3, that *Cole* teaches determining a range of intrinsic variation from the claimed plot of quiescent current. Not only does *Cole* lack the claimed plot of quiescent current from which the claimed range of intrinsic variation is determined, but also in column 10, lines 1-16 cited by the rejection, *Cole* teaches away from the claimed invention by identifying defective integrated circuits from time delay, not from quiescent current. Because *Cole* does not teach determining a range of intrinsic variation from the claimed plot of quiescent current, the modification of *Verhelst* by *Cole* proposed by the rejection fails to arrive at the claimed invention.

Further, suppose that *Cole* did teach determining a range of intrinsic variation from a plot of quiescent current

measured from the two supply lines *VDD* and *VSS*. The same current must flow in each of the supply lines *VDD* and *VSS*, because they are connected in series with the integrated circuit under test. Because the quiescent current must be the same in each of the supply lines *VDD* and *VSS*, there can be no intrinsic variation of quiescent current in a plot of quiescent current from the supply line *VDD* vs. quiescent current from the supply line *VSS*. Because there can be no intrinsic variation of quiescent current in a plot of quiescent current from the supply line *VDD* vs. quiescent current from the supply line *VSS*, the supposition that *Cole* teaches determining a range of intrinsic variation from a plot of quiescent current from the two supply lines *VDD* and *VSS* cannot be true.

Because *Verhelst* does not teach or suggest the claimed second supply voltage in addition to the supply voltage *VDD*, and because *Verhelst* does not teach or suggest the claimed measurement of quiescent current at a second supply voltage, and because *Cole* does not teach or suggest generating the claimed plot of quiescent current, and because *Cole* does not teach or suggest the claimed determination of a range of intrinsic variation from the claimed plot of quiescent current, the modification of *Verhelst* by *Cole* proposed by the rejection fails to arrive at the claimed invention. Because the modification proposed by the rejection fails to arrive at the claimed invention, Claims 1, 3, 5, 7, 9 and 11 are not obvious under 35 U.S.C. § 103(a).

Applicant respectfully requests examination and favorable reconsideration of Claims 1-16.

No additional fee is believed due for this

amendment.

Respectfully submitted,

Eric James Whitesell
Reg. No. 38,657

Address all correspondence to:
LSI Logic Corporation
1621 Barber Lane, M/S D-106
Milpitas, CA 95035-7458

Direct telephone inquiries to:
Timothy R. Croll
(408) 433-7625